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Madhusudan Ghosh received his B.Sc.(Physics), M.Sc.(Physics) and Ph.D.(Science) degree from Burdwan University, West Bengal, India in the year 1997, 1999 and 2013 respectively. At present he holds a faculty positions at the department of Physics, Govt General Degree College Singur, Hooghly, West Bengal, India. His research interest centres on field of synchronous communication system and nonlinear dynamics of discrete controlled systems. He has published about 9 research papers in inland and foreign journals and has contributed about 4 technical papers in national and international seminars and conferences.

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List of Journal Publications

(i) **M. Ghosh**, Dr A. Hati, Dr B. C. Sarkar, "*phase detector for data clock recover circuit*", Institute of Electrical Engineers, UK (2002), Vol: 38, No.: 04, pp: 161-163, 14th February, 2002

(ii) **M. Ghosh**, Dr A. Hati, Dr B. C. Sarkar, "*On improving the spectral purity of the regenerated clock signal in a data clock recovery circuit*", Indian Journal of Engineering and Material Science (IJEMS), Vol: 09, pp: 255-259, August, 2002

(iii) **M. Ghosh**, T. Banerjee and B. C. Sarkar , "*Design limitations and its effect in the performance of ZC1-DPLL*", ACEEE International Journal on Communication, Vol: 3, Issue: 1, pp: 48-52, 2012

(iv) **M. Ghosh**, T. Banerjee and B. C. Sarkar , "*Nonlinear Dynamics and Chaos in Second Order ZC1-DPLLs with Inherent Time Delay*", International Journal of Engineering and Advanced Technology (IJEAT), Vol: 01, no.-6, pp: 235-242, Aug, 2012

(v) **M Ghosh,** "*Performance Enhancement of Digital Phase Locked Loop (DPLL) Based FM Demodulator by Using of Variable Gain Control in the Negative Region of the Input Signal*", MAC Journal of Basic and Applied Sciences, Volume 2, No. 1, pp - 67-74, March 2015

(vi) **M Ghosh**, S. Dutta, "A Fast Acquisition Data Clock Recovery Circuit", MAC Journal of Basic and Applied Sciences, Volume 2, No. 1, pp - 111-116, March 2015

(vii) **M. Ghosh,** "*Improvement of the Performance of DPLL Based FM Demodulator by using of Variable Gain Control in the Positive Region of the Input Signal*", International Journal of Advanced Research in Electronics and Communication Engineering (IJARECE), Volume 4, Issue 5, pp - 1359-1362, May 2015

(viii) **M. Ghosh,** "*Additive Noise Response of Some Novel Phase Detector Based Charge Pump PLL Circuits; an Analytical and Simulation*", Indian Journal of Applied Research (IJAR), Volume 5, Issue 10, pp - 726-731, October 2015, ISSN No: 2249-555X

(ix) **M. Ghosh,** "*Nonlinear Dynamics and Chaotic Behavior of Delayed Digital Phase Locked Loop*", Scientific Voyage, Accepted for Volume 1, Issue 3, October 2015 ISSN No: 2395-5546